## **REMARKS**

This is intended as a full and complete response to the Office Action dated May 3, 2007 (hereinafter "the Office Action") having a shortened statutory period for response set to expire on August 3, 2007.

Claims 11 and 12 have been amended. Accordingly, claims 1-27 are presently pending. Entry of this amendment is respectfully requested to put the above-captioned application either in condition for allowance or better condition for appeal.

With regard to the response in the Office Action in view of Applicants' remarks, Applicants respectfully request the following additional remarks be considered. With reference to Section 2.1 of the Office Action, additional remarks regarding why U.S. Patent No. 5,920,600 ("Yamaoka") is distinguishable are provided below toward the end of the response to the rejection of claims 1-27. It should be particularly noted that in Yamaoka, an input clock is decoupled from providing an output clock during a synchronization mode. With reference to Section 2.2 of the Office Action, Applicants retain their position. Applicants believe the selection of these references and their combination to be improper hindsight reconstruction in the light of the claimed invention. The reasons for Applicants' position were previously made of record in the prior response to the rejection of claims 1-27 and are incorporated herein by reference for purposes of brevity. Notably, in Section 2.2 of the Office Action, reference is made to "Yokogawa et al."; however, Applicants assumed that the Examiner intended to make reference to "Yamaoka et al." and have interpreted the Office Action based on this assumption.

Claims 1-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,487,648 ("Hassoum") in view of U.S. Patent No. 5,625,580 ("Read") and in further view of Yamaoka. With this rejection, Applicants respectfully disagree, at least for the reasons previously made of record, which are incorporated by reference to this response to the rejection, and for the following additional reasons.

PATENT Conf. No.:7556

With regard to the third element of a prima facie case for obviousness and the remarks in Section 2.1 of the Office Action, Applicants provide the following additional remarks regarding Yamaoka. Applicants respectfully submit that what Yamaoka discloses is a stable phase selector that detects a stable phase timing based on a best phase fit of a multiphase clock to a pattern in a preamble of burst cell data in a synchronization mode decoupled from an input clock. (Ÿamaoka, at col. 19, line 3, to col. 21, line 5.)

Detector 163 in FIG. 28 of Yamaoka is for matching a preamble PR of a burst data cell. (Yamaoka, at col. 20, lines 11-22.) This synchronization is done using a multiphase clock 2011 from reset VCO 4A input to stable phase selector 16. (Yamaoka at col. 19, lines 11-26.) A reset signal 17 is used to cause the stable phase selector 16 to disable selection controller 6C. (Yamaoka, at col. 19, lines 55-63.) Accordingly, phase control input 2009 to reset VCO 4A is disabled, and VCO 4A runs at a frequency responsive to a frequency control voltage 2003. (e.g., Yamaoka, at col. 5, lines 22-37, with reference to col. 19, lines 27-36.) Notably, Section 2.1 of the Office Action in referring to Yamaoka at col. 11, lines 58-65, indicates that VCO 4 is masked so as not to input an "active" signal to phase control input 2009. Furthermore, it should be appreciated that input frequency control voltage 2003 is separate from input clock 2011. In short, output of multiphase clocks 2011 by reset VCO 4A when in a synchronization mode is decoupled from input clock 2011.

Claims 11 and 12 have been amended, and thus now all the independent claims recite an input clock used to provide an output clock. In contrast to Yamaoka, in each of the independent claims an input clock is used for providing an output clock, the latter of which is masked for clock stabilization. Notably, it stands to reason that if an input clock of Yamaoka is not stable, obtaining synchronization by use of multiphase clocks unrelated to such input clock does not achieve clock stabilization as claimed.

Accordingly, it is once again respectfully submitted that claims 1, 8, 11, 12, 13, 14, 24, and 27 are in condition for allowance and such allowance is respectfully requested. Furthermore, claims 2-7, 9-10, 15-23, and 25-26, which either directly or indirectly depend upon an allowable base claim, are likewise allowable.

PATENT Conf. No.:7556

## **CONCLUSION**

All claims should now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

Michael R. Hardaway Attorney for Applicants

Reg. No. 52,992

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 25, 2007.

Julie Matthews Name

Signature